Be prepared to debug a scan yield example:

* Does it look like a systematic or random defect?
  + Wafer mishandling? One time thing?
  + Wafer misprocessing? Tool issue?
  + How will it correlate to the product die?
* Does it affect Sail yield at different voltage corners?
* Is it the entire lot? Or just a few wafers?
* Does it affect both Sail 1 and Sail 2 in the same way?
* Is there any wafer regionality to the fails?
* Is there any slot level dependency?
* Are there any splits on the lot?
* What blocks are failing most often? Is there a pattern to them?
* What latches are on the blocks that are failing? Are they related?
* Where are the blocks located in the scan chain?
* What scan outs are failing more often on the block? Is it a specific scan chain that always fails?
* Do the block fails have regionality dependence?
* Do the block fails have voltage dependence?
* Is it random or systematic?

Process optimization for yield and power/performance

P metal residual stuck in m026 nfet, can fix by making PC CD bigger, which makes a longer channel device (slower performance) – reliability issue, cause issue long term because hard etch, softer etch means leaving stuff behind.

Demonstrate knowledge of ATE tests

* Stuck at 1, stuck at 0 test – feed in checkerboard twice inversed, slow speed, fails don’t affect next latches
* At speed (transition) tests – find slow to rise, slow to fall fails, feed in checkerboard and if the transition doesn’t happen or it happens at the wrong time, there’s a timing defect
* Path delay test -
* IDDQ Test – measure supply current (IDD) at the quiescent state (inputs are held at static value and circuit is not switching). Measure at different static states to see if there’s a defect that draws excess current.
* Toggle Test – not for defect detection. Try different circuit configurations fast, to make sure you can drive the latch to 1 or 0. Can be done fast so used for burn-in testing to cause high activity in the circuit.
* N-detect/ Embedded Multiple Detect (EMD)
* Deterministic Bridging
* Small-Delay Defects

ABIST (Array built in self test) – scan in instructions and it spits out results , LBIST (Logic built in self test)

In FA - Thermal detection, Photon Detection, shmoo many tests on a defect to see at what conditions it can actually pass park the chip at the boundary of pass and fail (scan a laser over to see what x,y location brings fail to a pass) <- CPA Critical Parameter Analysis

Latch up fails – catastrophic fails that turns on a stays on

Continuity test – short of open. Power supply set to 0v and pull current out of pad and measure voltage, see if the value is high or low to tell if short or open.

SRAM – ABIST, direct access to addresses to force write and read from pads. We have data pins

There’s a potential for addressing code issue where that’s broken and you only write to the same cells. BFM – have expected data output, log fails.

Advanced semiconductor technology node process integration knowledge

Physical structure, finfet, process limitations, PC CD, bridging, shifts, lithography related fails, CMP related, leaving liner behind, contacts – can’t dig deep enough to make contact. Stuff left over, or etched out. 2 different contats CA – source drain, CB on the gate, different levels – how to not over etch or under etch

WAT/eTest, Inline data analysis and correlation to yield

* Wafer Acceptance Testing (WAT) also known as Process Control Monitoring (PCM) data is data generated by the Fab at the end of manufacturing and generally made available to the fabless customer for every wafer.

Knowledge of Failure analysis techniques for speed path and systematic yield issue root cause

Scan ATPG and MBIST fail debug – scan diagnostics and bitmaps volume analysis

* (Automatic test pattern generation)